REMARKS

Claims 1-19 are pending in the subject application. Claims 1-6, 17, and 18 stand rejected under 35 USC §102(b). Claims 11, 16, and 19 stand rejected under 35 USC §103(a). Claim 18 further stands objected to and rejected under 35 U.S.C. § 112, second paragraph. Objections have been raised against the specification and several of the drawings. Claims 7-10 and claims 12-15 are objected to. Claims 1 and 18 have been amended.

The Applicants appreciate the Examiner's thorough examination of the subject application and respectfully request reconsideration of the subject application based on the above amendments and the following remarks.

35 U.S.C. § 112, SECOND PARAGRAPH REJECTIONS

The Examiner has objected to and rejected claim 18 under 35 USC 112, second paragraph as being indefinite for failing to particularly point out and distinctly claim the subject matter that the Applicants regard as their invention. Claim 18 has been amended. Accordingly, the Applicants believe that the grounds for rejection are now moot.

35 U.S.C. § 102(b) REJECTIONS

The Examiner has rejected claims 1-6, 17, and 18 under 35 USC 102(b) as being anticipated by U.S. Patent Number 4,996,523 to Bell, et al. ("Bell" or the "Bell Reference"). The Applicants respectfully traverse these rejections in view of the above amendments and for reasons detailed below.

The Bell reference discloses a matrix-type electro-luminescent storage display element having a plurality of memory cells interposed between the data and signal lines for driving MOS switches. See, e.g., Bell, Abstract. The Examiner asserts that

Bell teaches a memory element that is arranged by connecting at least two inverters to each other in a loop manner, wherein an output of an output inverter, which functions as an output end of the memory element, is directly connected to one end of the optical modulation element. The Applicants respectfully disagree.

Specifically, according to the disclosure,

> FIG. 4 illustrates a second circuit implementation for a memory cell 22_n. A MOS transistor 31 has its drain electrode connected to receive the signal B_n, its gate electrode is connected to receive the ROW signal and its source electrode is connected to the inputs of CMOS inverters 33 and 35. The outputs from inverter 33 and inverter 35 are connected to the gate electrode of an associated MOS transistor 24.

Id., col. 4 lines 12-19 (Emphasis added). In short, the source electrode, e.g., TFT, provides input to both inverters and the output of both inverters provides input to the MOS transistor, e.g., OLED. Thus, an output of an output inverter, which functions as an output end of the memory element, is not directly connected to one end of the optical modulation element.

In contrast, as shown in FIG. 1 of the present invention, the output of the "input inverter" 11a is provided as input to the "output inverter" 11b and the output of the "output inverter" 11b is provided as feedback to the input of the "input inverter" 11a. Thus, the TFT 13 of the present invention only provides input to the "input inverter" 11a and only the output of the "input inverter" 11a is connected to the OLED 12. See, e.g., Specification, page 16, lines 7 to page 18, line 4. Accordingly, the Bell reference teaches away from the invention as claimed and therefore, does not anticipate claim 1 of the present invention or any of the claims depending therefrom.

Thus, it is respectfully submitted that, claims 1-6, 17, and 18 are not anticipated by Bell and, further, satisfy the requirements of 35 U.S.C. 100, et seq., especially § 102(b). Accordingly, claims 1-6, 17, and 18 are allowable. Moreover, it is

respectfully submitted that the subject application is in condition for allowance. Early and favorable action is requested.

35 U.S.C. § 103(a) REJECTIONS

The Examiner has rejected claim 11 under 35 USC 103(a) as being unpatentable over Bell in view of U.S. Patent Number 5,945,972 to Okumura, et al. ("Okumura" or the "Okumura Reference") and claims 16 and 19 under 35 USC 103(a) as being unpatentable over Bell in view of U.S. Patent Number 6,369,788 to Yamazaki, et al. ("Yamazaki" or the "Yamazaki Reference"). The Applicants respectfully traverse these rejections in view of the above amendments and for reasons detailed below.

Claim 11

For the same reasons that the present invention is not anticipated by the Bell reference, it is also not made obvious thereby. Moreover, the Okumura reference cannot make up for the deficiencies of the Bell reference. Specifically, Okumura does not teach, mention or suggest a memory element having an output of an output inverter, which functions as an output end of the memory element, that is directly connected to one end of the optical modulation element.

Thus, it is respectfully submitted that, claim 11 is not made obvious by Bell in view of Okumura and, further, satisfies the requirements of 35 U.S.C. 100, et seq., especially § 103(a). Accordingly, claim 11 is allowable. Moreover, it is respectfully submitted that the subject application is in condition for allowance. Early and favorable action is requested.

Claims 16 and 19

For the same reasons that the present invention is not anticipated by the Bell reference, it is also not made obvious thereby. Moreover, the Yamazaki reference cannot make up for the deficiencies of the Bell reference. Specifically, Yamazaki does

not teach, mention or suggest a memory element having an output of an output inverter, which functions as an output end of the memory element, that is directly connected to one end of the optical modulation element.

Thus, it is respectfully submitted that, claims 16 and 19 are not made obvious by Bell in view of Yamazaki, further, satisfy the requirements of 35 U.S.C. 100, et seq., especially § 103(a). Accordingly, claims 16 and 19 are allowable. Moreover, it is respectfully submitted that the subject application is in condition for allowance. Early and favorable action is requested.

The Applicants believe that no additional fee is required for consideration of the within Response. However, if for any reason the fee paid is inadequate or credit is owed for any excess fee paid, you are hereby authorized and requested to charge Deposit Account No. **04-1105**.

Respectfully submitted,

Date: January 26, 2004

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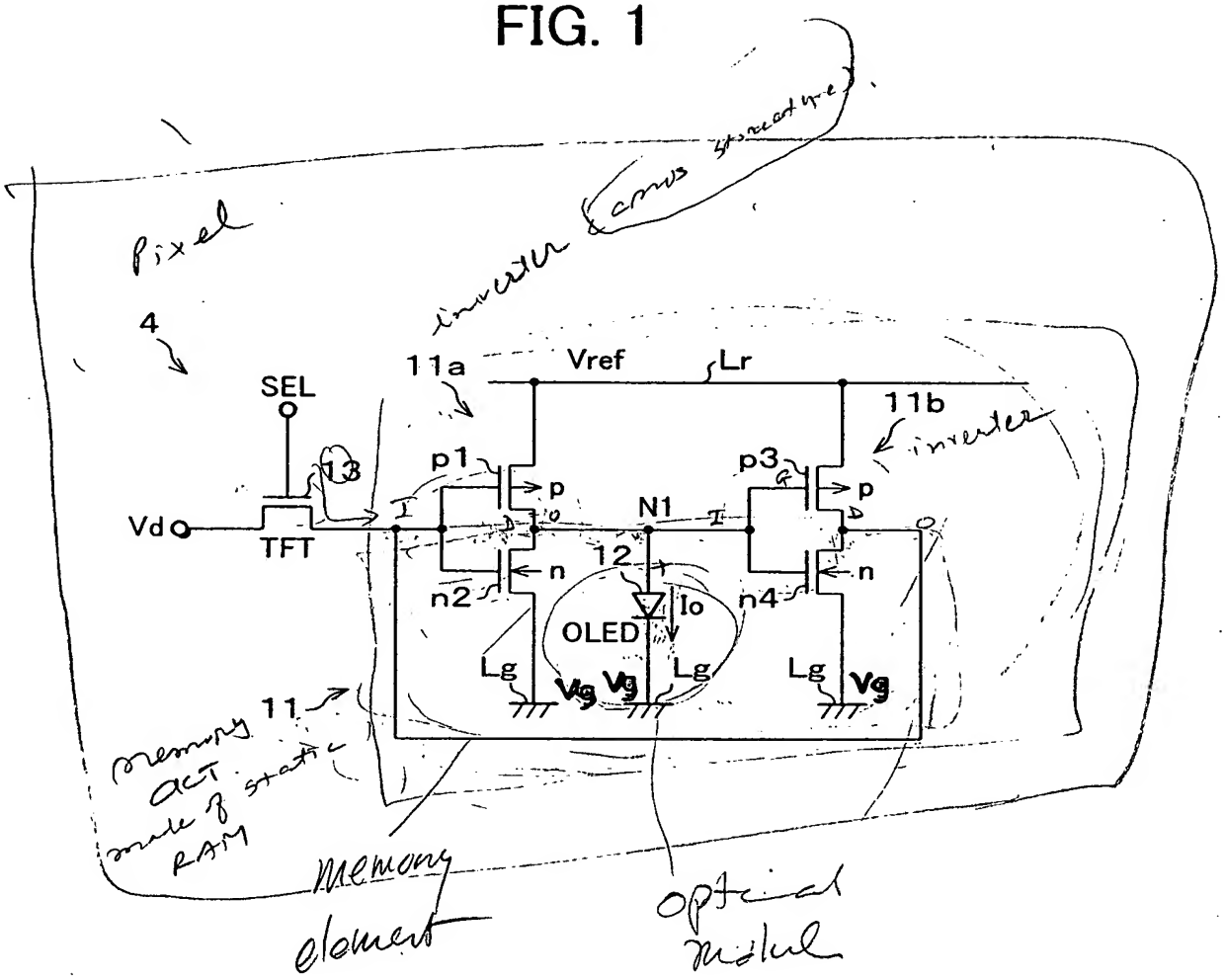
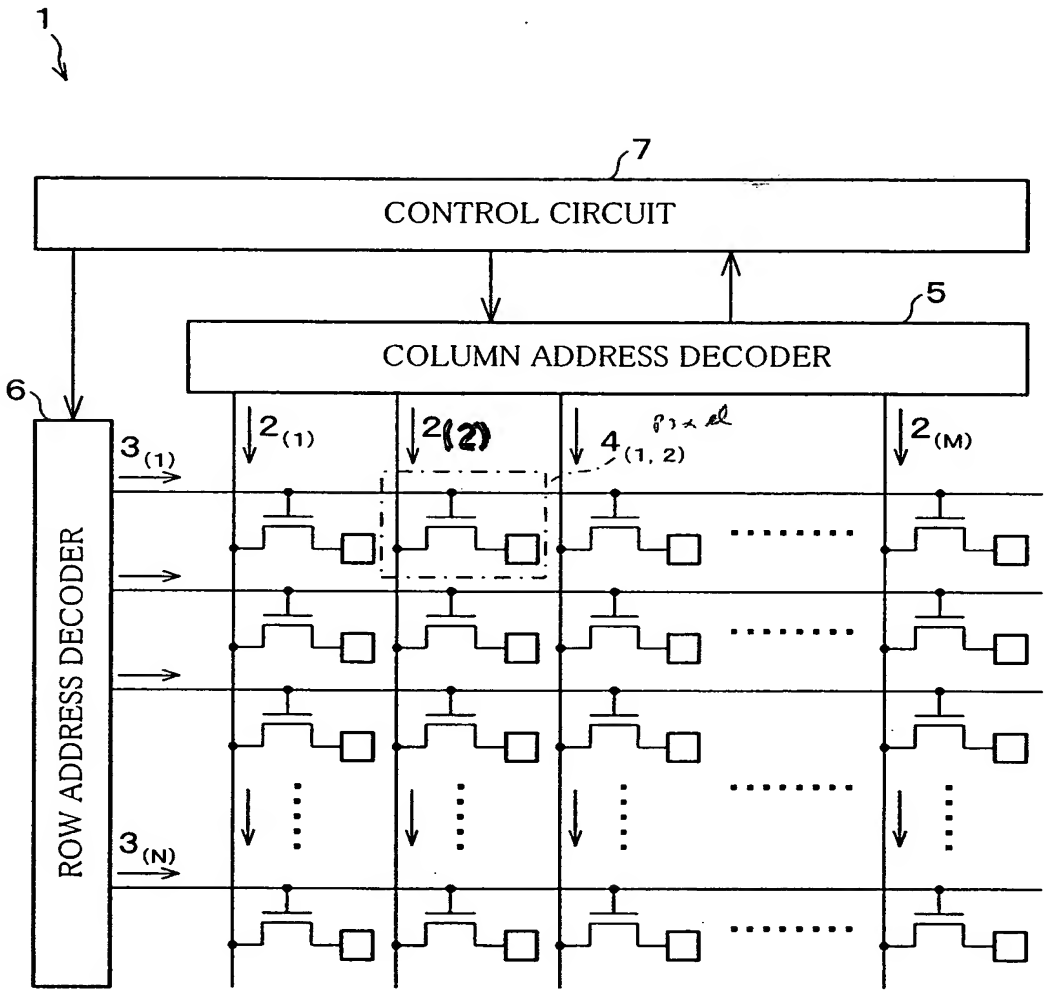
FIG. 1



11a or 11b

FIG. 2



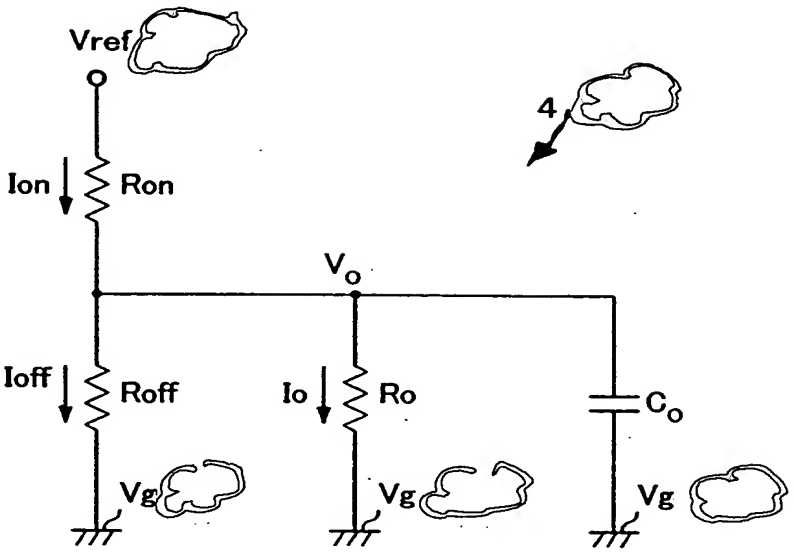


FIG. 4A

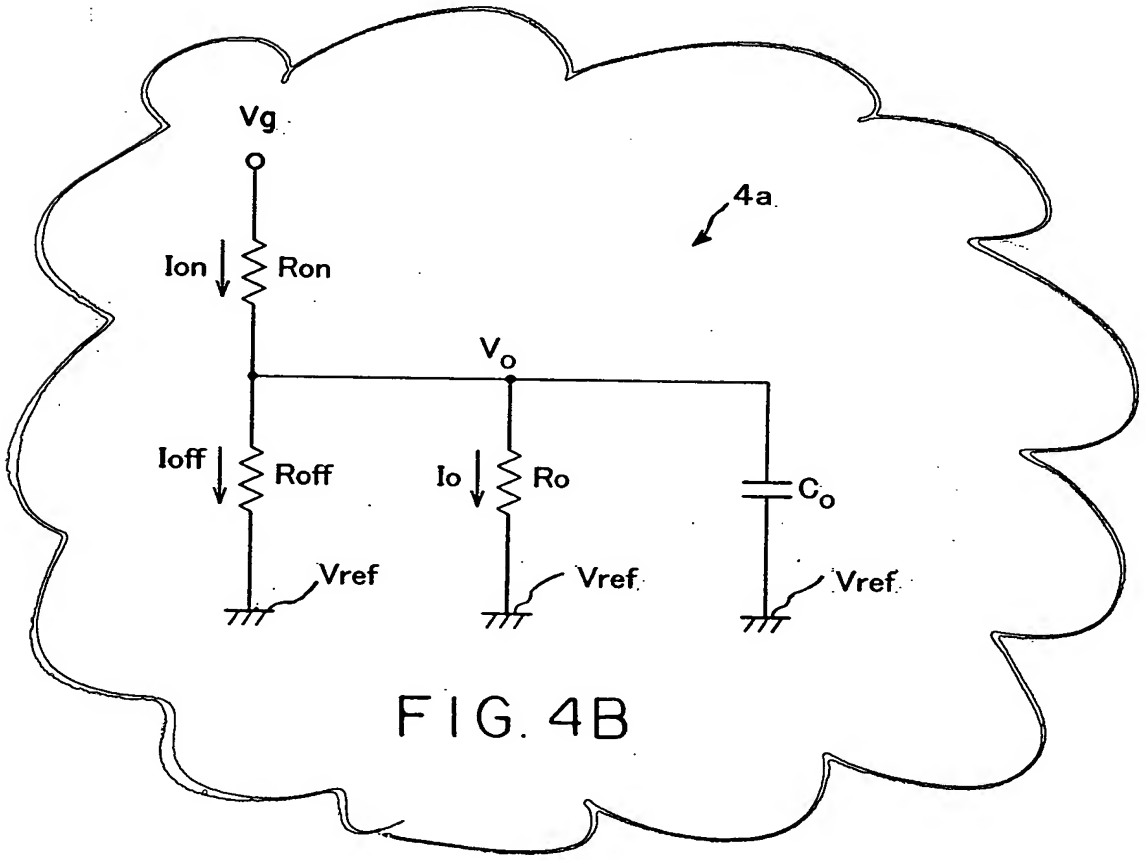


FIG. 4B

FIG. 18 PRIOR ART

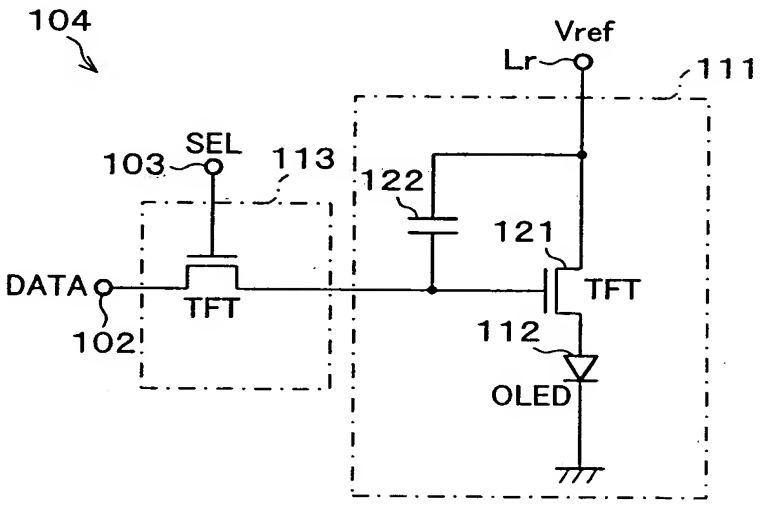


FIG. 19 PRIOR ART

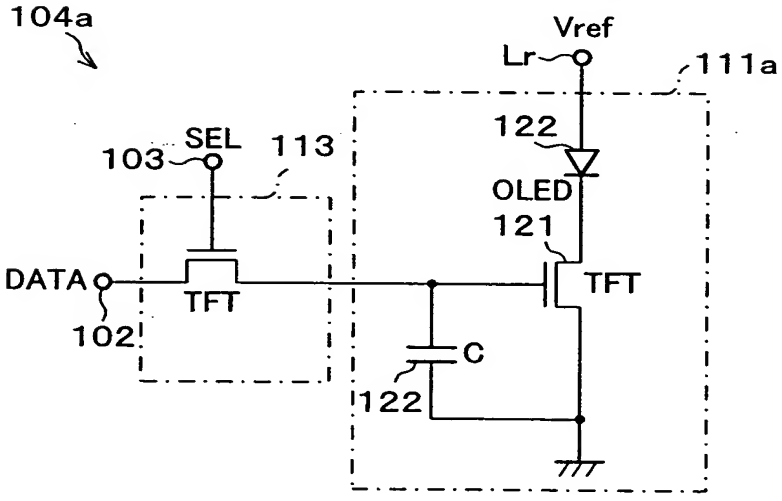


FIG. 20 PRIOR ART

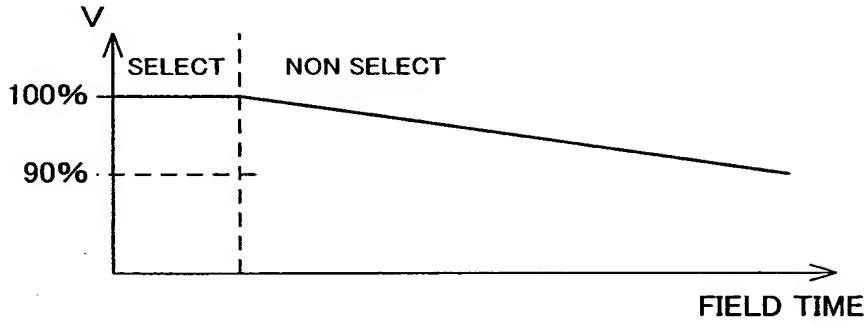


FIG. 21 PRIOR ART